On-Chip Adaptive VDD Scaled Architecture of Reliable SRAM Cell With Improved Soft Error Tolerance

Neha Gupta, Ambika Prasad Shah, *Member, IEEE*, Rana Sagar Kumar, Tanisha Gupta, Sajid Khan, and Santosh Kumar Vishvakarma, *Member, IEEE*

***Abstract*—Negative bias temperature instability (NBTI) is the major reliability issue which affects many parameters such as threshold voltage, mobility, and leakage current. The threshold voltage of the PMOS transistor increases due to NBTI with stress time, which degrades the circuit performance. In this article, we have proposed a novel reliable data-dependent low power 10T SRAM cell, which is highly stable and free from half select issues. We investigated all the circuit simulations using 65nm CMOS technology. The proposed 10T cell has a higher critical charge and lower soft error rate (SER) as compared to other SRAM cells. To better assess, we introduced a bit read failure (BRF) at read operation and observed that the BRF of the proposed 10T cell is significantly reduced as compared to the other considered SRAM cells at 0.15V supply. The leakage power, write power-delay-product, and read power-delay-product of the proposed 10T cell is 0.1×, 0.21×, and 3.13×, respectively as compared to the conventional 6T cell at 0.4V supply. The proposed cell offers 4×, 1.15× and 1.66× higher read, hold and write margin, respectively, as compared to 6T cell at 0.4V supply voltage. The simulation result shows that the HSNM, WSNM, and RSNM are decreased by 0.31%, 0.13%, and 0.08%, respectively, with the proposed 10T cell while 6T cell reduces 3.21%, 0.43%, and 8.62%, respectively, after 10 years of stress time. We have also introduced an on-chip adaptive VDD scaled reconfigurable architecture compared to the conventional array architecture design to reduce 97.04% and 92.17% hold power of unselected cells during read and write operation of the selected cell, respectively for the proposed 10T cell.**

***Index Terms*—Negative bias temperature instability (NBTI), reliability, soft error rate (SER), data-dependent low power, bit read failure (BRF).**

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Neha Gupta, Sajid Khan, and Santosh Kumar Vishvakarma are with the Nanoscale Devices, VLSI Circuit and System Design Laboratory, Discipline of Electrical Engineering, Indian Institute of Technology Indore, Indore 453552, India (e-mail: phd1701202008@iiti.ac.in; skvishvakarma@iiti.ac.in).

Ambika Prasad Shah is with the IC reliability and security lab, Discipline of Electrical, Indian Institute of Technology Jammu, Jammu 181221, India.

Rana Sagar Kumar is with the Intel Technology India Private Ltd., Bangalore 560017, India.

Tanisha Gupta is with the School of Electronics, DAVV Indore, Indore 452001, India.

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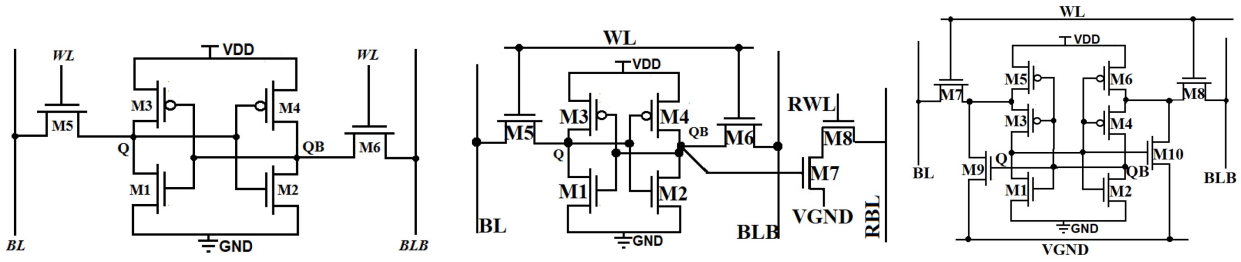
I. Introduction

THE NANOSCALE CMOS technology is demanded to be more reliable, optimized, fault-tolerant, and low power in the present and future electronic devices. With the aggressive down-scaling of CMOS technology, aging has become a major issue to affect circuit performance, which requires special concern and monitoring in modern technology nodes. In the recent technology nodes, the impact of multiple temporal degradations like Hot Carrier Injection (HCI), Bias Temperature Instability (BTI), Time-Dependent Dielectric Breakdown (TDDB) are more affected. These temporal degradations increase the threshold voltage and delay while reducing the leakage current and carrier mobility [1]. Due to the degradation of performance parameters, it is required to overcome the aging effects on the MOS devices. The MOS transistors are affected by negative BTI as well as positive BTI. However, non-high-k metal transistor, 65nm, or before, shows that the NBTI effect in PMOS is more dominant as compared to NBTI and PBTI effects on the NMOS transistor as well as PBTI effect on PMOS transistor. Hence for simplicity, only NBTI in PMOS has been considered in most of the analysis [2], [3].

Along with the BTI, the reliability issues are also influenced by the single event upsets (SEUs) [4], [5]. The SEUs are caused by alpha particles and cosmic neutrons, which are generated from the packaging materials and radiation, respectively. These energetic alpha particles strike on the circuit or storage node and generate faults or logical errors. Such errors are referred to as soft errors [6], [7]. The soft error is measured by the critical charge (Q_{crit}) of the most sensitive node in the circuit, and the critical charge has an exponential relationship with the soft error rate (SER), which indicates the SER should be low for the higher value of critical charge [8].

In most electronic devices, SRAM consumes more power with the technology scaled down. Therefore, the SRAM cells need to be considered for the power analysis and the reliability challenges. The supply voltage and critical charge is the essential parameter for the reliability analysis because the SRAM cells have a sensitive circuit. The conventional 6T SRAM cell is more pretended by the cosmic radiations, which increases the storage failure problem and reduces the noise margin [9], [10].



(a) (b) (c)

Fig. 1. Reference SRAM cell structures (a) Conventional 6T SRAM cell (b) 8T cell [11] (c) PPN10T cell [12].

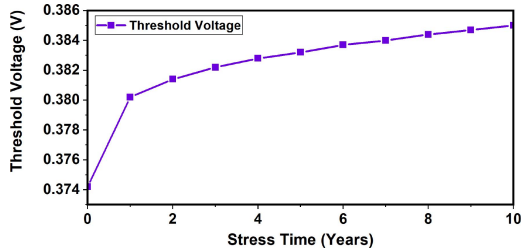


Fig. 2. Threshold voltage variation of PMOS transistor with different stress time.

To overcome the issues with the conventional 6T cell, a new approach is proposed to isolate the storage node from the read decoupled path. This approach (read decouple) improves the read noise margin and overcomes the issue of read disturbance in the circuit. The read decoupled circuit mitigates the write/read conflict, but two extra NMOS transistors in the read path increase the current during read condition [11]. The problem of read decoupled 8T cell is resolved by using two stacked PMOS transistors in PPN10T [12]. Stacking transistor reduces the leakage power consumption and also isolates the write and read operation. In PPN10T cell, the circuit has lower leakage power due to the stacking combination, but the cell's limitation has a higher delay during read and write operation.

In this article, we proposed a novel, reliable data-dependent low power 10T SRAM cell architecture to resolve all issues faced by state-of-art cell designs [13]. Hereafter, The proposed 10T cell is referred to with the name of "D^{2}LP10T". The proposed D^{2}LP10T cell has a higher critical charge and lowers SER as compared to conventional 6T, 8T [11], and PPN10T [12] cell, which is suitable for the error-tolerant applications. To access the novelty of the D^{2}LP10T cell, we propose a figure of merits (FOM) as a compound performance matrix. The FOM is considered an important parameter for the SRAM cell and observed that the FOM of the proposed D^{2}LP10T cell is reasonably higher as compared to other SRAM cells.

In this article, an on-chip adaptive VDD scaled reconfigurable architecture is also proposed. In this architecture, the supply selection circuit gives the output to control cell supply for all the operations and optimize power consumption. The other objectives of our study are:

- Examine the effect of NBTI for PMOS transistors under the stress condition and variation with a threshold voltage.
- Data-dependent low power 10T SRAM cell is proposed with improved reliability and reduced soft error rate (SER).
- Methodology and expression have been derived for the critical charge, SER and bit read failure (BRF), and analyze various other parameters such as leakage power, write power, read power, and stability.
- An on-chip adaptive VDD scaled reconfigurable architecture is proposed to reduce the overall power dissipation using VDD scaling, and an algorithm is developed for better understanding.
- The hold power is calculated for the unselected rows, and the result is compared with the conventional array for both 6T cell and D^{2}LP10T cell.

The rest of the paper is organized as follows: In Section II, we discuss the NBTI effect on the 6T SRAM cell and describe the operation of the proposed reliable 10T SRAM cell in Section III. In Section IV, we describe the analysis methodology and simulation results of the different SRAM cells are discussed in Section V. Section VI explains the on-chip adaptive VDD scaled reconfigurable architecture and algorithm design followed by the conclusions in Section VII.

II. NBTI Effect on 6T SRAM Cell

NBTI occurs in the PMOS transistor when the gate-to-source voltage becomes negative supply voltage, then the PMOS goes into a stress phase. Stress phase breaks Si-H bonds at Si/SiO_2 interface which is trapped into the oxide layer [14], [15]. The change in PMOS threshold voltage due to the stress can be expressed as [16], [17]:

$$\triangle V_{TH(Stress)} = A_{NBTI} \times t_{ox} \times \sqrt{C_{ox}(V_{DD} - V_T)} \times e^{\frac{V_{DD}-V_T}{t_{ox}E_0} - \frac{E_a}{kT}} \times t_{stress}^{0.25} \quad (1)$$

where A_{NBTI} is the aging dependent constant, t_{ox} is the oxide thickness. C_{ox} is the gate capacitance, t_{stress} is the stress time, and E_0, E_a are the constant values. The change in threshold voltage due to stress is not permanent. After the stress phase is removed, a recovery phase is initiated which occurs when the V_{GS} becomes logic 0 and hence recovers the threshold voltage change [18]. However, all of the trapped charges cannot be recovered in the recovery phase; therefore, the threshold voltage increases with time. The increase of V_{TH} after considering both the stress and recovery phases are given below [16], [17]:

$$\triangle V_{TH} = \triangle V_{TH(Stress)} \times \left(1 - \sqrt{\eta \times \frac{t_{Recovery}}{t_{Stress} + t_{Recovery}}}\right) \quad (2)$$

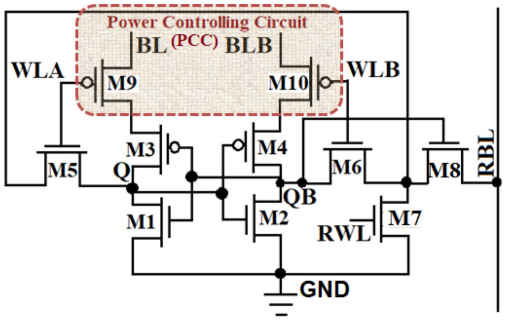


Fig. 3. Schematic of Proposed D^{2}LP10T SRAM cell.

where $t_{Recovery}$ and t_{Stress} are the recovery time and stress time, respectively. η is a constant with value of 0.35 [16].

Fig. 1 (a) shows the typical 6T SRAM cell, where the effect of the NBTI generates unpredictability in circuit performance and reduces the circuit existence. The value of threshold voltage increases with the stress time in the PMOS transistor, as shown in Fig. 2. The increment of the threshold voltage affects noise margin, leakage current, propagation delay, and failure probability with the aging time.

III. Proposed Reliable D^{2}LP10T SRAM Cell

Fig. 3 and TABLE I show the schematic design and control signal status of the proposed D^{2}LP10T SRAM cell, respectively [13]. The construction and features of the proposed D^{2}LP10T cell are as follows:

- It consists of two extra PMOS switches in the pull-up network, which is powered by bit lines instead of direct supply, and this connection is called the power controlling circuit (PCC).
- In power controlling circuit (PCC), M9 and M10 transistors are controlled by WLA and WLB signals, which cut-off the M9 and M10 transistors from the bit lines during the read phase and resolve the half select issue.
- The D^{2}LP10T cell enhances the soft error immunity because the power controlling transistors are forcefully turned ON by the control signals WLA and WLB, and the PCC is independent of the storage node, which makes the higher critical charge. Therefore, the power controlling circuit is the strength of the proposed cell.
- Series connected transistors are used to enhance stability and reduce leakage power of the cell.
- Read decoupling approach is used to separate the read and write path, which enhances the read stability and resolves the read/write trade-off without any power penalty.

To perform read mode of operation, the major involving transistors are M7 and M8. Assuming that all the bit lines (BL, BLB and RBL) are precharged to logic 1, RWL is activated while WLA and WLB control signals are disabled, as shown in TABLE I. Where RBL either remains precharged or discharges to VDD, depending on whether QB stores 0 or 1, respectively. During write 0 operations, WLA and BLB are at logic 1, and WLB and BL are set to logic low, while RWL is connected to logic 1 as shown in TABLE I. Therefore, the left inverter is completely cut-off from the bit line (BL), and M6

TABLE I
Control Signals for Proposed D^{2}LP10T Cell

Control Signals	Operation			
	Write 0	Write 1	Read	Hold
WLA	1	0	0	0
WLB	0	1	0	0
RWL	1	1	1	0
BL	0	1	1 (floating)	1 (floating)
BLB	1	0	1 (floating)	1 (floating)

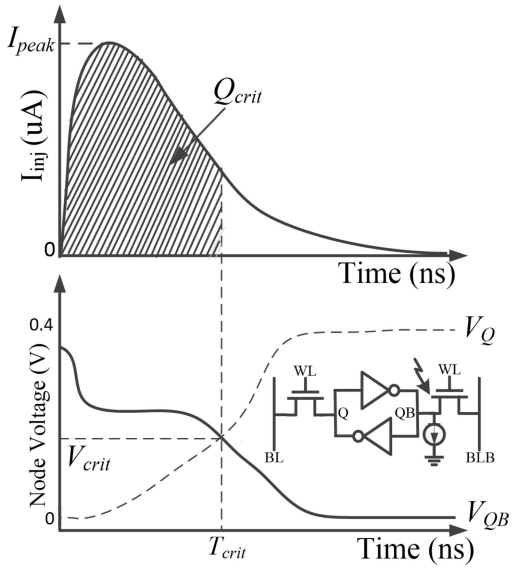


Fig. 4. Graphical representation of critical charge.

is also cut off due to WLB signal. Thus, the storage node Q is effortlessly discharged through M5 and M7. Similarly, for write 1 operation, node QB is easily discharged through the M6 and M7, and consequently, 1 is written at the storage node Q. All the access transistors are cut-off during standby mode. The control signals are also disabled, while bit lines are floating or precharged to high. It provides floating storage nodes, which maintain its data at the storage node and also reduce the leakage power.

The power consumption is reduced due to the supply voltage scaling, but the stability and critical charge are also reduced. So VDD scaling is a challenging task if we consider all the above parameters simultaneously. However, the proposed design provides an effectively higher critical charge, lower soft error rate, and less bit read failure without degrading the stability.

IV. Analysis Methodology

In this section, we defined the methodology to determine the different parameters which we evaluated in this article.

A. Critical Charge

The critical charge is calculated at the most sensitive node of the memory cell, when the radiation particles strike at that node. Therefore a double exponential current pulse is injected

into the most sensitive node of the memory cell to determine the critical charge (Q_{crit}) [5], [6].

Fig. 4 describes the critical charge and calculates the minimum magnitude and duration of the injected current pulse that is sufficient to flip the data in the sensitive nodes of the memory cell. Hence, Q_{crit} is computed by integrating the current pulse from 0 to T_{crit}.

$$Q_{\text{crit}} = \int_0^{T_{\text{crit}}} I_{\text{inj}}(t)dt \tag{3}$$

where I_{inj}(t) is the injected current pulse at the sensitive node for a single event upset (SEU), and T_{crit} is the time to flip the stored data due to the injection of current pulse equivalent to the particle strike at node [19].

B. Soft Error Rate

The soft error rate (SER) of the circuit can be examined from the critical charge. The critical charge is estimated as the minimum amount of charge collected by the sensitive node to flip the stored data. The soft error rate determines the possibility of flipping the stored data due to particle strike and it is mainly the function of critical charge and drain diffusion area as given below [20].

$$SER = F \times K \times \left(A_{d,n} \int_{Q_{crit,n}}^{\infty} f_Q(q)dq + A_{d,p} \int_{Q_{crit,p}}^{\infty} f_Q(q)dq \right) \tag{4}$$

$$SER = F \times K \times \left(A_{d,n} e^{-\frac{Q_{crit,n}}{Q_{S,n}}} + A_{d,p} e^{-\frac{Q_{crit,p}}{Q_{S,p}}} \right) \tag{5}$$

where $f_Q(q) = \frac{1}{Q_S} e^{-\frac{q}{Q_S}}$, K is the technology-independent fitting parameter and F is total neutron flux. $A_{d,n}$, $Q_{crit,n}$, $Q_{S,n}$ and $A_{d,p}$, $Q_{crit,p}$, $Q_{S,p}$ are the drain diffusion area, critical charge and charge collection efficiency of NMOS and PMOS transistor, respectively. Hence, the SER is exponentially dependent on the critical charge, which confirms that the higher value of Q_{crit} translates lower SER [20].

The soft error rate ratio ($SERR_{\#}$) is calculated to analyze the soft error rate (SER) of the considered SRAM cells normalized to the 6T cell [21]. Therefore, the SERR is calculated using the given equation:

$$SERR_{\#} = \frac{SER_{\#}}{SER_{6T}} \tag{6}$$

$SER_{\#}$ is the soft error rate of all the reference SRAM cells like 6T, 8T, PPN10T and the proposed D^{2}LP10T cell, which is calculated using equation (5).

C. Bit Read Failure

In the SRAM cell design, stability directly depends on the supply voltage. However, bit read failure (BRF) is defined as a probability that the RSNM of SRAM cells is less than zero or no stable condition, so this cell is known as an unreadable cell. The ratio of the unreadable cell to overall cell capacity is the bit read failure, which is an important metric to estimate the minimum supply voltage required for the SRAM cell [22], [23].

Assuming that the SNM follows the rules of Gaussian distribution, when we want to estimate the error rate of SRAM cells, we estimate the SNM probability density function. Therefore, the BRF is calculated with the probability at estimated RSNM is less than zero, as shown in equation (7) [24]

$$BRF = \int_{-\infty}^{0} \frac{1}{\sqrt{2\pi}\sigma_{SNM}} exp\left(-\frac{(V_{SNM} - \mu_{SNM})^2}{2\sigma_{SNM}^2} \right) \tag{7}$$

where, σ_{SNM} is the standard deviation, μ_{SNM} is the mean of the distribution, and V_{SNM} is the supply voltage at near-threshold voltage, which is used for SNM calculation during read operation.

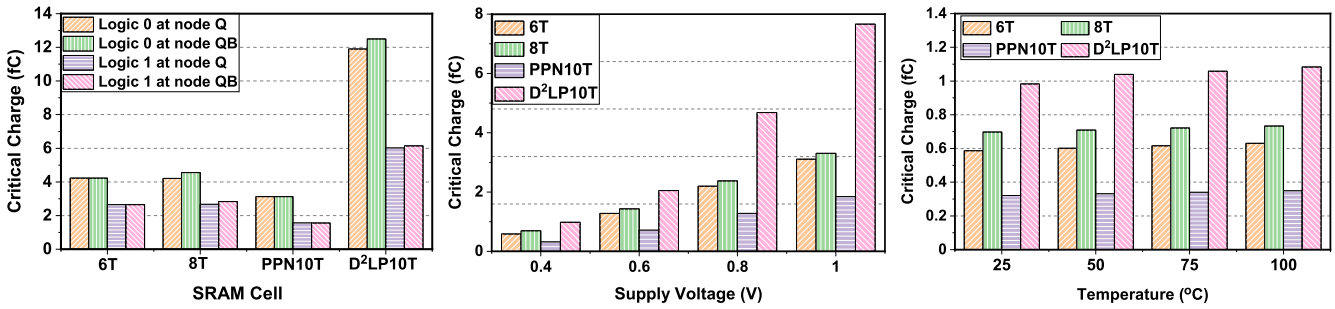
V. Simulation Results and Discussion

The D^{2}LP10T cell and other reference circuits have been designed and simulated using 65nm CMOS technology using a specific aspect ratio. Where the simulation is performed by Cadence and HSPICE-MOSRA model. The performance parameters of D^{2}LP10T cell are compared with 6T, read decoupled 8T [11], PPN10T [12], as shown in Fig. 1. Various parameters performance, stability, and reliability are examined and compared with all the considered SRAM cells.

A. Critical Charge

The simulations were conducted using the double-exponential current pulse, where rise and fall time constant are 1ps and 50ps, respectively [21]. Fig. 5(a) shows the critical charge analysis at node Q and QB for considered SRAM cells at 0.9V supply voltage and 25°C temperature. From the result, the higher value of the critical charge is observed when logic 0 is stored at the node Q or QB. Moreover, the Q_{crit} is lower for all the SRAM cells at logic high and considered for further critical charge and soft error rate analysis. Where, the storage node QB with logic 1 is considered as a sensitive node because drain diffusion area is more at node QB as compared to node Q. The result also shows that the Q_{crit} of the 6T and 8T cell is same at node Q due to affected transistors are equal and the Q_{crit} of 8T cell is slightly higher at node QB due to one extra M7 transistor in 8T cell as compared to the 6T cell.

Further, Fig. 5(b) and (c) show the critical charge at node QB as high logic for the considered SRAM cells. From Fig. 5(b) it is observed that, the critical charge of the proposed cell is increased by 2.46×, 2.31× and 4.14× at 1.0V supply and 25°C temperature as compared to 6T, 8T and PPN10T cell, respectively. Moreover, Fig. 5(c) shows the critical charge of proposed cell is increased by 1.71×, 1.47× and 3.09× at 0.4V supply and 100°C temperature as compared to 6T, 8T and PPN10T cells, respectively. Because the PMOS transistors M9 and M10 are forcefully turned ON by the control signals WLA and WLB and the power controlling circuit (PCC) is independent from the storage nodes, which becomes higher critical charge. Whereas in the other reference circuits, the pull-up network is only controlled by the storage nodes Q and QB. Therefore when the α particles strike on the storage node, it will directly impact the transistor conditions and reduce the critical charge. This is the main reason that the critical charge of the proposed circuit is much higher as compared to other



(a) (b) (c)

Fig. 5. Critical charge analysis (a) at node Q and QB (b) of different supply voltage variations and (c) different temperature variations for SRAM cells.

TABLE II
PARAMETERS FOR SER ESTIMATION

VDD (V)	0.9
$f_{D,n}$	0.123
$f_{D,p}$	0.088
$\mathbf{Q}_{S,n}$ **(fC)**	5.72
$\mathbf{Q}_{S,p}$ **(fC)**	2.88

TABLE III
DRAIN DIFFUSION AREA A_{dn} AND A_{dp} AT NODE Q AND QB

SRAM Cell	**at node Q**		**at node QB**	
	$\mathbf{A}_{dn}$ **(μm^2)**	$\mathbf{A}_{dp}$ **(μm^2)**	$\mathbf{A}_{dn}$ **(μm^2)**	$\mathbf{A}_{dp}$ **(μm^2)**
6T	0.072	0.014	0.072	0.014
8T	0.072	0.014	0.079	0.014
PPN10T	0.028	0.028	0.028	0.028
D^{2}LP10T	0.043	0.072	0.050	0.072

reference circuits. From the above discussions, we conclude that the proposed D^{2}LP10T cell has better soft error hardening due to a higher critical charge in voltage and temperature variations.

B. Soft Error Rate

The parameter values are given in TABLE II, that are scaled from 100nm [25], [26] to 65nm. The drain diffusion area $A_{d,n}$ and $A_{d,p}$ at the sensitive nodes Q and QB are shown in TABLE III. From the result, it is observed that the proposed cell has smaller $A_{d,n}$ because NMOS area size is lesser than the 6T and 8T cells. However, $A_{d,p}$ of the proposed cell is larger because PMOS area size is larger as compared to other SRAM cells. The detailed description of aspect ratio will be discussed in Section V-I.

The soft error rate ratio ($SERR_{\#}$) is calculated using equation (5) and (6) for the considered SRAM cells normalized to the 6T cell at 0.9V supply voltage and 25°C temperature, as shown in Fig. 6. The results show that the proposed D^{2}LP10T cell has least $SERR_{\#}$ by 0.35×, 0.34× and 0.43× as compared to the 6T, 8T and PPN10T cell, respectively at the sensitive node QB. The soft error will be induced when a radiation event occurs close enough to a sensitive node such that Q_S is greater than Q_{crit} [4]. Therefore, the proposed cell has no soft error because Q_{crit} is greater than Q_S as shown in Fig. 5(a) and TABLE II. Hence we conclude that the proposed D^{2}LP10T cell is robust against the soft error.

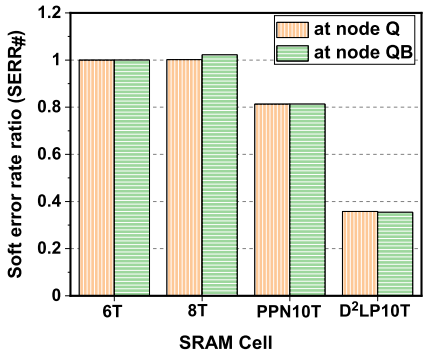


Fig. 6. Soft error rate ratio at 0.9V supply and 25°C temperature condition.

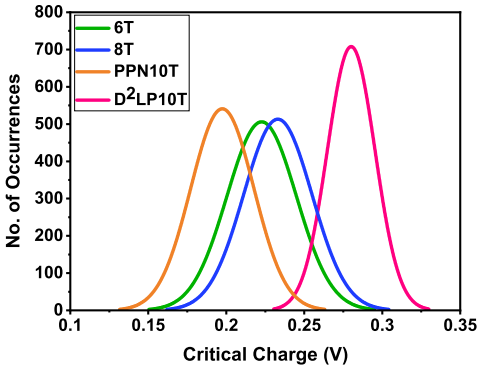


Fig. 7. 5000 Monte Carlo simulated statistical distribution plot of critical voltage for different SRAM cells.

C. Process Variation Analysis

We analyzed the critical voltage (V_{crit}) for the analysis of soft error resilience and process variations on various SRAM cells. The critical voltage is defined as the voltage when the voltages at the storage nodes (Q and QB) are equal, as shown in Fig. 4. The V_{crit} is examined using 5000 Monte Carlo simulations including the process and mismatch variations with $\pm 3\sigma$ deviations as illustrated in Fig. 7. In each simulation run, it calculates every parameter randomly according to a statistical distribution model [14], [27]. The Monte-Carlo simulation is performed using Cadence ADE-XL, which considers both the process and mismatch variations. The simulation result shows that the proposed D^{2}LP10T cell has the highest mean and the lowest variability as compared to other cells [28].

TABLE IV
PARAMETERS OF CRITICAL VOLTAGE STORAGE NODE

SRAM Cells ↓	Critical Voltage (V_{crit})		
	Mean (μ)	Standard deviation (σ)	Variability (σ/μ)
6T	0.22	0.022	0.1
8T	0.23	0.022	0.095
PPN10T	0.19	0.020	0.105
D^{2}LP10T	0.28	0.015	0.053

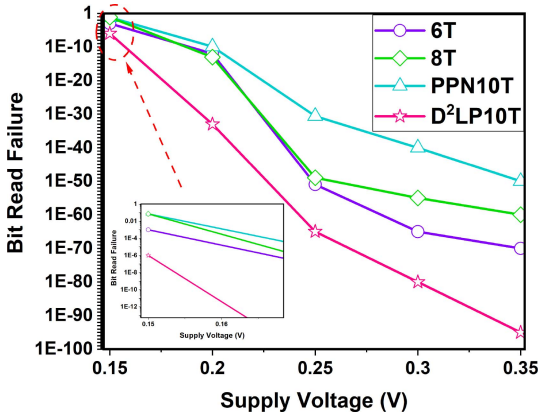


Fig. 8. Bit read failure (BRF) during the read operation of different SRAM cells with supply voltage variation.

TABLE IV shows the mean (μ), standard deviation (σ) and variability (σ/μ) of the critical voltage at higher voltage and temperature. The results show that the proposed D^{2}LP10T cell is increased by 1.27×, 1.22× and 1.47× mean value and reduced by 0.68×, 0.68× and 0.75× variability as compared to 6T, 8T and PPN10T cell, respectively at 1.0V supply and 100°C temperature. Hence, from the above discussions, we concluded that the effect of process variations are less in the proposed D^{2}LP10T cell.

D. Bit Read Failure

In this section, we determine the impact of bit read failure (BRF) in the SRAM array using 5000 Monte Carlo simulation during the read operation. Fig. 8 shows the bit read failure of the different cells with various supply voltages. The result shows that the BRF continuously decreases when the supply voltage increases and the proposed 10T cell is significantly reduced compared to the other considered SRAM cells at 0.15V supply. It is because the chance of read failure reduces when the supply voltage increases. From the comparative results, we analyze that the on-chip reconfigurable architecture is suitable for the scaled supply (VDD$_S$) approach at the read operation, that we will further discuss in Section VI. Therefore, the bit read failure is very less in the case of the proposed D^{2}LP10T cell at lower supply voltage.

E. Leakage Power

The sub-threshold leakage power is a serious issue with the technology scaled-down, and supply voltage reduces. As we know that most of the time, the major part of the cache memory is in the standby mode, and therefore leakage power contributes a large portion of total power consumption in an SRAM cell [29], [30]. Supply voltage scaling is one of the practical approaches to minimize the leakage power of the circuit.

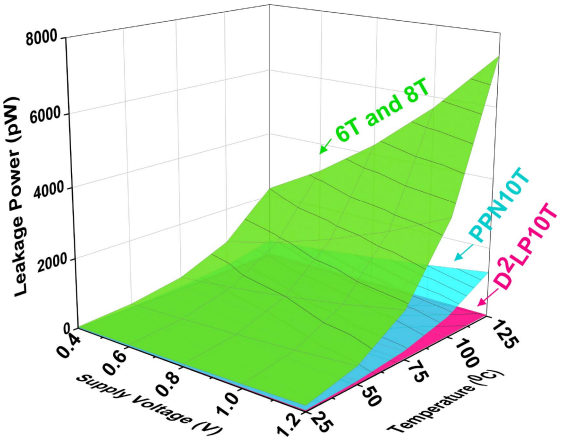


Fig. 9. Comparison of leakage power of different SRAM cells at different supply voltages and temperature variations.

Fig. 9 shows the least amount of leakage power in the D^{2}LP10T cell with the variations of supply voltage and temperature. The proposed D^{2}LP10T cell involves the stacking transistors and data-dependent power supply in the cross-coupled inverter pair, which reduces the enormous amount of leakage power in the cell. Nevertheless, the proposed D^{2}LP10T cell consumes 89.96%, 90.27%, and 67.47% less leakage power at 0.4V supply and 25°C temperature as compared to 6T, 8T, and PPN10T SRAM cell, respectively. Whereas the proposed D^{2}LP10T cell consumes 99.42%, 99.42%, and 96.76% less power at 1.2V supply and 125°C temperature as compared to 6T, 8T, and PPN10T cell, respectively. The reduction in leakage power implies to degrade the overall power consumption of the proposed cell, which is significantly used in the embedded memory applications [31].

F. Write and Read Active Power

We also analyze the power dissipation during read and write operations of all the considered SRAM cells. The write power of D^{2}LP10T cell has 97.75%, 98.34% and 71.70% less for write 0 operation, as compared to 6T, 8T and PPN10T cell, respectively as shown in Fig. 10(a). The huge amount of power saving in the write operation is because of the power controlling circuit used in the proposed cell, which cut-off one side of the inverter and save a significant amount of power.

In Fig. 10(b), the read power of the proposed D^{2}LP10T cell is less than 6T and PPN10T cell but higher than the 8T cell because of the separate read path is present in the 8T and proposed D^{2}LP10T cell. From the result, it is observed that the D^{2}LP10T cell is reduced by 0.89×, 0.96×, and 0.72× as compared to 6T, 8T, and PPN10T, respectively at 0.4V supply voltage. Hence, the proposed D^{2}LP10T cell has lower active power and is suitable for energy-efficient applications.

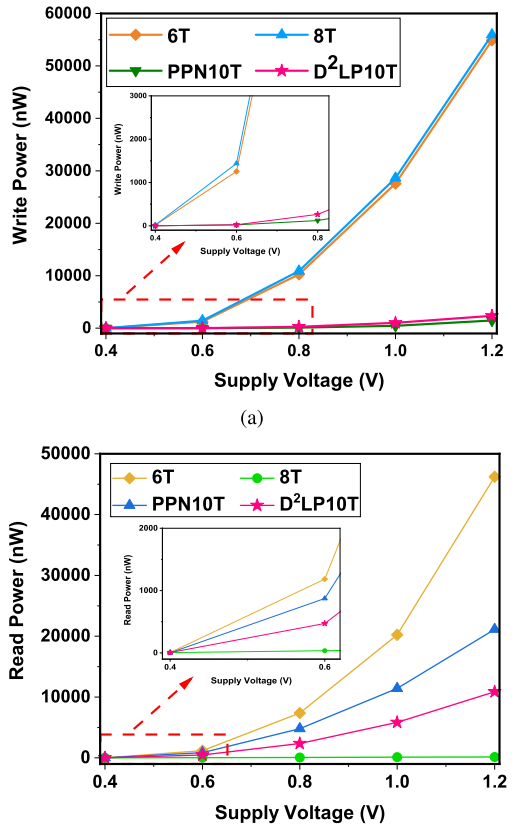


Fig. 10. Power dissipation of various SRAM cells at different supply voltage for (a) Write operation (b) Read operation.

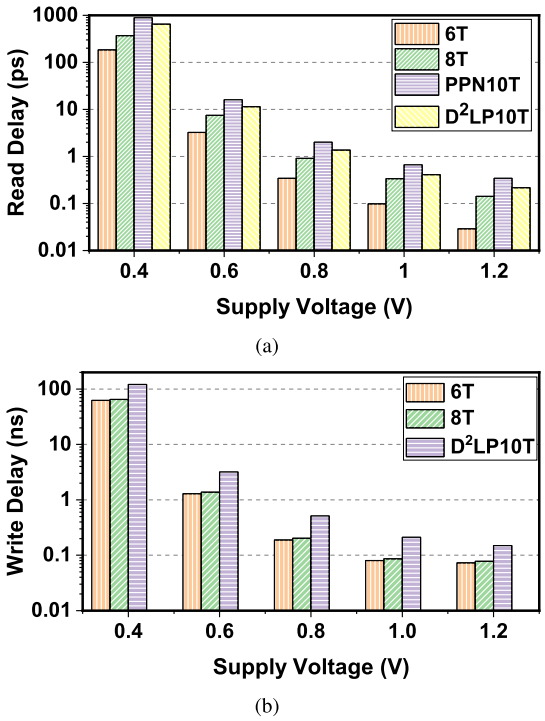


Fig. 11. (a) Read delay and (b) write delay of various SRAM cells at different supply voltages.

TABLE V
POWER DELAY PRODUCT (PDP) OF DIFFERENT SRAM CELLS AT 0.4V SUPPLY VOLTAGE

SRAM Cells	Read PDP (aJ)	Write PDP (fJ)
6T	0.93	0.14
8T	1.71	0.19
PPN10T	5.48	0.13
D^{2}LP10T	2.92	0.03

G. Read and Write Delay

The read delay is estimated as the time between activation of RWL signal and the discharging of RBL by 50mV from its initial value [32]. From Fig. 11(a), it can be seen that the proposed D^{2}LP10T cell sacrifices in terms of read speed as the read delay are 3.51× and 1.76× higher than the 6T and 8T cell and 0.73× lower than the PPN10T cell at 0.4V supply voltage. However, the read delay of the proposed cell is high due to increased bit line capacitance and more time to discharge the bit line capacitance than 6T and 8T cells. The read delay of the proposed cell and 8T cell is almost the same because the similar read access path is connected to the read bit line, showing the equivalent bit line capacitance present in these cells. Although, the read power of the D^{2}LP10T cell is improved as compared to considered SRAM cells. Therefore, the overall read performance is evaluated using read energy in terms of read power and delay product (read PDP), as shown in TABLE V.

Write 1 delay is calculated as the time between the activation of RWL and the storage node Q reading up to 90% of VDD. Similarly, write 0 delay is measured as the time between the activation of RWL and the storage node Q reading up to 10% of VDD [33]. The proposed cell suffered from the write speed by 1.94× and 1.86× as compared to 6T and 8T cells at 0.4V supply voltage, as shown in Fig. 11(b). The PPN10T cell has not been considered for the write performance because the delay of PPN10T cell is 99.17× higher as compared to the D^{2}LP10T cell, so it is not necessary to compare in Fig. 11(b). Although, the proposed D^{2}LP10T cell provides better write power, as discussed in the previous section. Therefore, the overall write performance of the considered SRAM cells is presented in terms of write energy as shown in TABLE V.

H. Stability

We have analyzed the static noise margin of the different SRAM cells using the butterfly curve method, where the stability is determined by the side length of the largest square, which is best fitted on the minimum lobe of the butterfly curve [10], [34]. In such a way, we have calculated the RSNM, HSNM, and WSNM at 0.4V supply, as shown in Fig. 12. In the proposed D^{2}LP10T cell, the RSNM is improved by 4×, 1.15× and 1.58×; WSNM by 1.66×, 1.43× and 1.08×; HSNM by 1.15×, 1.15× and 1.58×as compared to 6T, 8T, and PPN10T cell, respectively. The enhancement of WSNM is due to the combination of the series-connected transistors in the pull-up network and the increment of RSNM is due to isolating the read decoupled path from the storage node in the proposed circuit, whereas the conventional 6T cell is more susceptible towards the noise because of the voltage divider

TABLE VI
SNM (mV) ANALYSIS OF 6T AND D^{2}LP10T CELL WITH DIFFERENT STRESS TIME

Stress Time (Year)	RSNM		HSNM		WSNM	
	6T	D^{2}LP 10T	6T	D^{2}LP 10T	6T	D^{2}LP 10T
0	31.3	125.5	109	125.6	138.2	229.5
2	30.76	125.48	108.3	125.52	138.08	229.44
4	30.22	125.46	107.6	125.44	137.96	229.38
6	29.68	125.44	106.9	125.36	137.84	229.32
8	29.14	125.42	106.2	125.28	137.72	229.26
10	28.6	125.4	105.5	125.2	137.6	229.2

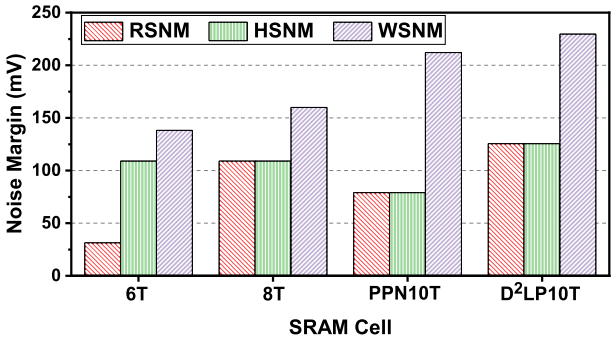


Fig. 12. Static noise margin during all operation models for various SRAM cells at 0.4V supply voltage.

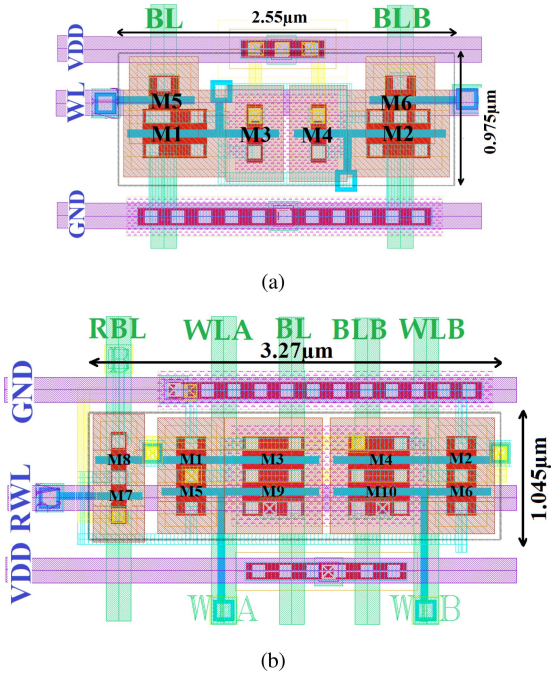


Fig. 13. Layout of (a) 6T cell and (b) Proposed D^{2}LP10T cell.

formation in the read path, which remains connected to the storage node. Moreover, the stacking connection in the cross-coupled inverters of the proposed D^{2}LP10T circuit increases the equivalent resistance and helps to control the noise, which is affecting the stored data at the storage nodes during read and hold operation [33].

The stability of write, hold, and read is also analyzed by performing pre-stress and post-stress conditions using threshold voltage change, which is given in equation (1). Moreover, we have considered the DC stress for the simulation because the effect of NBTI in DC stress is more severe than AC stress. Because the AC stress is having both stress and recovery phases, whereas DC has only stress conditions. TABLE VI shows the read, hold and write stability at 25°C temperature and 0.4V supply voltage for 6T and D^{2}LP10T cells with different aging time. The stability of the SRAM cells depends on the stress time and it decreases with the stress time because the threshold voltage of PMOS transistor (M3) increases, causing the trip point voltage to be reduced for the right inverter circuit [35]. The simulation result shows that the HSNM, WSNM, and RSNM of 6T cell is decreased by 3.21%, 0.43% and 8.62%, respectively, while the proposed D^{2}LP10T cell is reduced by 0.31%, 0.13%, and 0.08%, respectively after 10 years of stress time. The small degradation shows other temporal degradation components.

I. Cell Area Comparison and Aspect Ratio

The physical layout structure of conventional 6T and proposed D^{2}LP10T SRAM cells in 65nm standard CMOS technology are shown in Fig. 13. The aspect ratio of the conventional 6T cell consists of cell ratio (pull-down to access transistor ratio) and pull-up ratio (pull-up to access transistor ratio), which is 2 and 0.5, respectively, with minimum pull-up transistor sized by 120nm width and 60nm length for 65nm CMOS technology node. In the 8T cell [11], read decoupled transistors are sized by minimum width and length with 120nm and 60nm, respectively and the remaining transistor sizing is the same as 6T cell. While PPN10T cell sizing is taken from [12]. Whereas, the cell ratio and pull-up ratio of the D^{2}LP10T cell is 1 and 2.5, respectively, with a minimum size of read decoupled transistors and double-sized of access transistors. Therefore, the 6T cell area and the proposed D^{2}LP10T cell is 2.48μm^2 and 3.41μm^2, respectively and the proposed cell consumed 1.37× area than the 6T cell. The larger size of all PMOS transistors for pull-down NMOS transistors is used to degrade the conductivity which is appeared by the series-connected transistors and also enhance the hold stability.

J. Figure of Merit (FOM)

The essential parameters of the SRAM cell at the near-threshold region are listed in TABLE VII. The results demonstrate that the proposed cell has the lowest PDP (power-delay-product), leakage power and soft error with slightly higher area overhead as compared to other considered cells. Moreover, the stability is higher as compared to reference cells at 0.4V supply and 25°C temperature.

Further, the figure of merits (FOM) is an important factor in motivating their relative utility and performance parameters to determine SRAM applications [35]. There are many significant parameters to defined FOM, such as read and write PDP, leakage power, SERR, estimated area, and stability, as shown in TABLE VII. Since stability should be maximum, it is placed at the numerator in the equation. Whereas the write and read PDP, leakage power, SERR and estimated area should

TABLE VII
PERFORMANCE COMPARISON OF STATE-OF-ART SRAM CELLS AT 0.4V SUPPLY VOLTAGE

SRAM Cells ↓	Performance Parameters									
	Critical Charge (fC)	Normalised SERR	RSNM (mV)	HSNM (mV)	WSNM (mV)	Leakage power (pW)	Write PDP (fJ)	Read PDP (aJ)	Normalised Area	FOM
6T	1.042	1	31.3	109	138.2	16.14	0.14	0.93	1	1
8T [11]	1.127	1.022	109	109	160	16.66	0.19	1.71	1.15	1.32
PPN10T [12]	0.505	0.813	79	79	212	4.98	0.13	5.48	2.01	0.95
D^{2}LP10T	1.267	0.354	125.5	125.5	229.5	1.62	0.03	2.92	2.16	143.3

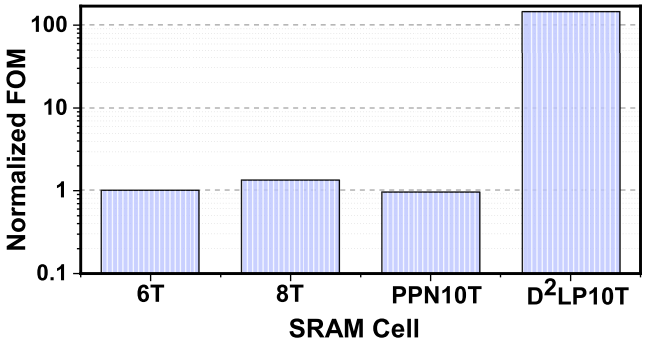


Fig. 14. Figure of merit for different SRAM cells at 0.4V supply voltage.

be minimum, so they placed at the denominator in the FOM formula. Here, the novel FOM equation is given below:

$$FOM = \frac{RSNM_n \times HSNM_n \times WSNM_n}{SERR_n \times WPDP_n \times RPDP_n \times LP_n \times A_n} \quad (8)$$

where, $RSNM_n$, $HSNM_n$, $WSNM_n$, $SERR_n$, $WPDP_n$, $RPDP_n$, LP_n and A_n are the normalized values of read SNM, hold SNM, write SNM, soft error rate ratio, write power-delay-product, read power-delay-product, leakage power and estimated area, respectively. All the values are normalized with the 6T SRAM cell. Fig. 14 shows that the FOM of the proposed D^{2}LP10T cell is 143.3× higher as compared to 6T cell. FOM includes all the essential parameters of the circuit, so the D^{2}LP10T circuit is best suited for high performance, low power circuits with the nominal area penalty.

VI. PROPOSED ON-CHIP ADAPTIVE VDD SCALED ARCHITECTURE

In conventional memory architecture, all the cells are configured simultaneously on full swing supply voltage, which leads to overhead power consumption [36]. However, the majority of cells remain idle during hold state, which contributes a considerable amount of leakage power consumption where the contribution of leakage power is substantial in terms of the total power consumption in any digital circuits [29]. In the idle case, the leakage power should be as low as possible, which is overcome by the scaled supply approach and verified in Section V-E that the leakage power is reduced when the supply voltage is scaled down. Therefore, supply scaling is one of the best techniques to resolve leakage power consumption, especially when the cell is in an idle condition.

An on-chip adaptive VDD scaled reconfigurable architecture is proposed by choosing the supply voltage according to the selection of cell conditions, as shown in Fig. 15. In this architecture, we proposed a novel supply selection circuitry which generates full supply (VDD) and scaled supply (VDD$_S$) according to the selection of SRAM cells with the help of address lines. The output VDD selects the entire one row, which has a selected cell, and the output VDD$_S$ selects the entire unselected rows in idle state. In this way, we have drastically reduced the leakage power of entire unselected rows with scaled supply (VDD$_S$). The full swing supply (VDD) is used to write and read operation successfully, and scaled supply (VDD$_S$) is used for the unselected cell to hold the data in idle mode. The selection of the supply voltage is carried out by row and column decoder circuit, to address lines and selects the individual cell. This scheme reduces the overall power consumption to a great extent as compared to conventional memory array architecture. The detailed flow of on-chip adaptive VDD scaled architecture is given in Algorithm 1.

A. Hold Power Consumption

The hold power equation is given below for the n × n array architecture. The given equation shows how many times the hold power is affected by the conventional architecture, using full swing supply. The hold power for the reconfigurable architecture is given by equation (9), as shown at the bottom of the page, where n × n is the no. of cells in column × row in the array. When the n × n array is used, the total supply voltage of conventional architecture is given by n×n×VDD and on-chip adaptive VDD scaled reconfigurable architecture is given by (n × (n − 1) × VDD$_S$+ n × 1 × VDD).

$$Hold\ power = \frac{Unselected\ n \times (n-1)\ array\ with\ scaled\ supply}{Full\ VDD\ supply\ of\ entire\ n \times n\ array} \quad (9)$$

$$Power\ Reduction = \frac{(n \times n \times VDD) - (n \times (n-1) \times VDD_S + n \times 1 \times VDD)}{n \times n \times VDD} \quad (10)$$

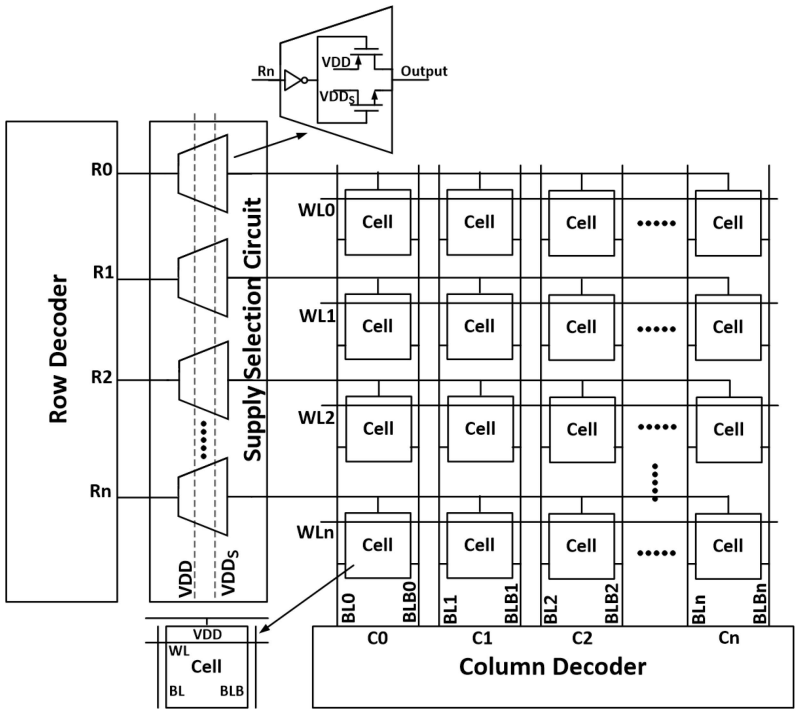


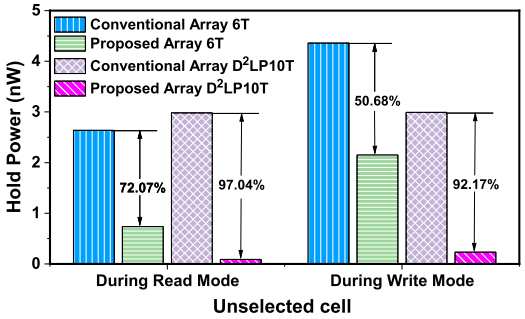
Fig. 15. Proposed on-chip adaptive VDD scaled reconfigurable architecture.

The total power reduction of on-chip adaptive VDD scaled reconfigurable architecture for hold power is given by equation (10), as shown at the bottom of the previous page.

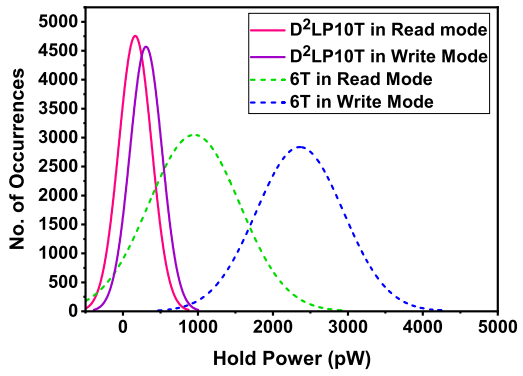
The on-chip adaptive VDD scaled reconfigurable architecture is applied in both conventional 6T and proposed D^{2}LP10T cells. The read and write operation is performed in the selected cell, and hold power is calculated for unselected cells, simultaneously, as shown in Fig. 16. Since when we write or read data to the one selected cell, the other unselected cells have an idle state and the hold power on that unselected cells in the unselected rows with the help of scaled supply VDD_S is calculated.

Fig. 16(a) shows the hold power of unselected rows when we read or write data to the selected cell at 1.2V supply voltage. The proposed on-chip VDD scaled array, and a conventional array is designed and calculated the hold power for conventional 6T cell and proposed D^{2}LP10T cell in 4 $\times$ 4 arrays. The result shows that the proposed array for 6T cell consumes 72.07% and 50.68% lower power during read and write operation, respectively, as compared to conventional array for 6T. Similarly, the proposed D^{2}LP10T cell consumes 97.04% and 92.17% lower power during read and write mode, respectively, as compared to the conventional array of D^{2}LP10T cell.

Fig. 16(b) shows the statistical distribution of mismatching and process variations for the hold power using 5000 Monte-Carlo simulations with $\pm 3\sigma$ deviations. In each simulation run, it calculates every parameter randomly according to a statistical distribution model. The Monte-Carlo simulation is performed using Cadence ADE-XL, which considers both the process and mismatch variation. The simulation result shows that the D^{2}LP10T cell has the highest mean and lowest



(a)



(b)

Fig. 16. Hold power dissipation of unselected cell in write and read operation at 1.2V supply voltage (a) comparison of conventional array and proposed scaled array (b) Statistical distribution plot of 5000 Monte-Carlo simulation for 6T and proposed cell using proposed scaled architecture.

standard deviation as compared to 6T cell during read as well as write mode at 1.2V supply voltage. From Fig. 16(b), it is also observed that the hold power of unselected cells is

Algorithm 1 On-Chip Adaptive VDD Scaled Reconfigurable Memory Architecture

```
if Operation = Cell selection then
  Row Decoder (R_n) ← Row address
  Column Decoder (C_n) ← Column address
  if Operation = Write then
    R_n ← logic '1'                    //Row decoder output
    VDD ← Logic high                   //Selected signal
    VDD_S ← Logic low                  //Unselected signal
    Cell supply ← VDD                  //Write data for selected cell
  else
    if Operation = Read then
      R_n ← logic '1'                  //Row decoder output
      VDD ← Logic high                 //Selected signal
      VDD_S ← Logic low                //Unselected signal
      Cell supply ← VDD                //Read data for selected cell
    else
      if Operation = Hold then
        R_n ← logic '0'                //Row decoder output
        VDD ← Logic low                //Unselected signal
        VDD_S ← Logic high             //Selected signal
        Cell supply ← VDD_S            //Hold for unselected cells
      end if
    end if
  end if
end if
```

almost similar in the proposed D^{2}LP10T cell during read and write operation. Whereas, the hold power of an unselected cell differs in the conventional 6T cell, when read and write operation is performed in the selected cell. Hence, it is concluded that the proposed D^{2}LP10T cell consumes the least amount of hold power as compared to 6T cell when proposed scaled architecture is used.

VII. Conclusion

In this article, we analyzed the impact of soft error and NBTI on reliable SRAM cells with scaled supply. The bit read failure suggested that VDD could be scaled down even at 0.15V for an accurate result when the proposed D^{2}LP10T cell is used. We also examined the cell stability, where hold, write, and read SNM is decreased by 0.31%, 0.13%, and 0.08%, respectively after 10 years of stress time for the proposed D^{2}LP10T cell and 3.21%, 0.43%, and 8.62%, respectively for the conventional 6T cell. Further, for the better outlook of the proposed cell, we demonstrated the critical charge of the proposed D^{2}LP10T cell is increased by 2.46×, 2.31×, and 4.14× as compared to 6T, 8T and PPN10T cell at 1.0V and 25°C, whereas the proposed D^{2}LP10T cell has the least soft error rate. The $SERR_{\#}$ is reduced by 0.35×, 0.34×, and 0.43× as compared to the 6T, 8T, and PPN10T cell, respectively at 0.9V supply voltage and 25°C operating temperature. As a consequence, we can conclude that the proposed D^{2}LP10T cell has the highest figure of merits that is 143.3× higher as compared to 6T cell and the overall performance is improved, and the proposed D^{2}LP10T cell is reliable with soft error tolerance and has less effect of NBTI. Further, we proposed an on-chip adaptive VDD scaled reconfigurable architecture to reduce 97.04% and 92.17% hold power of unselected cells during read and write operation of the selected cell, respectively as compared to the conventional array architecture design.

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Neha Gupta received the B.E. degree in electronics and telecommunication engineering from RGPV University Bhopal, India, in 2014, and the M.E. degree in electronics engineering from the Institute of Engineering and Technology, Devi Ahilya University, Indore, India, in 2017. She is currently pursuing the Ph.D. degree in electrical engineering with the Indian Institute of Technology Indore, India. Her current research interests include reliability analysis of digital circuits, low power and reliable SRAM design, and low power high performance digital circuit designs.

Ambika Prasad Shah (Member, IEEE) received the B.E. degree in electronics and telecommunication engineering and the M.E. degree in electronics engineering from the Institute of Engineering and Technology, Devi Ahilya University, Indore, India, in 2009 and 2015, respectively, and the Ph.D. degree from the Electrical Engineering Department, Indian Institute of Technology Indore, India, in 2019.

Before joining Ph.D. degree, he was an Assistant Professor with the Electronics and Telecommunication Engineering Department, Institute of Engineering and Technology, Devi Ahilya University from 2010 to 2016. He worked as a Postdoctoral Fellow with the Institute for Microelectronics, TU Wien, Vienna, Austria, from January 2019 to March 2020. He is currently working as an Assistant Professor with the Electrical Engineering Department, Indian Institute of Technology Jammu, India. He has authored/coauthored more than 43 research papers in peer reviewed international journals and conferences. His current research interest includes reliability analysis of digital circuits, fault tolerant circuits, and low power high performance digital circuit designs. He is a Lifetime Member of IAENG and an Associate Member of UACEE.

Rana Sagar Kumar received the B.E. degree in electronics engineering from the Maharaja Sayahirao University of Baroda, and the M.Tech. degree in VLSI design and nanoelectronics from the Indian Institute of Technology, Indore, India. He is currently with Intel Technology India Private Ltd., Bengaluru, India, as a CAD Engineer. His current research interest includes Low power, reliable SRAM designs, and high-performance digital designs.

Tanisha Gupta received the B.E. degree in electronics and communication engineering from Medi-Caps University, Indore, India, in 2017. She is currently pursuing the M.Tech. degree in embedded systems and VLSI with the School of Electronics, Devi Ahilya University, Indore. She is also pursuing internship from STMicroelectronics, Greater Noida, India, in her second year of course work. Her current research interest includes low power high performance analog circuit design for memories, and low power SRAM and DRAM design.

Sajid Khan received the bachelor's degree in electronics and communication from the Holkar Science College, Indore, India, in 2011, and the master's degree in electronics and communication from the School of Electronics, Devi Ahilya Vishwavidyalaya, Indore, in 2013. He is currently pursuing the Ph.D. degree in electrical engineering with IIT Indore, Indore. His research interests include security of Internet of Things, low power, reliable, and security circuit design.

Santosh Kumar Vishvakarma (Member, IEEE) received the B.Sc. degree in electronics from the University of Gorakhpur, Gorakhpur, in 1999, the M.Sc. degree in electronics from Devi Ahilya Vishwavidyalaya, Indore, India, in 2001, the M.Tech. degree in microelectronics from Punjab University, Chandigarh, India, in 2003, and the Ph.D. degree from the Indian Institute of Technology Roorkee, India, in 2010. From 2009 to 2010, he was with University Graduate Center, Kjeller, Norway, as a Postdoctoral Fellow under European Union project "COMON." He is currently an Associate Professor with the Department of Electrical Engineering, Indian Institute of Technology Indore, India, where he is leading Nanoscale Devices and VLSI Circuit and System Design Laboratory. His current research interests include nanoscale devices and circuits, reliable SRAM designs, multigate and multifin MOSFETs, and tunnel FETs and their circuit applications.