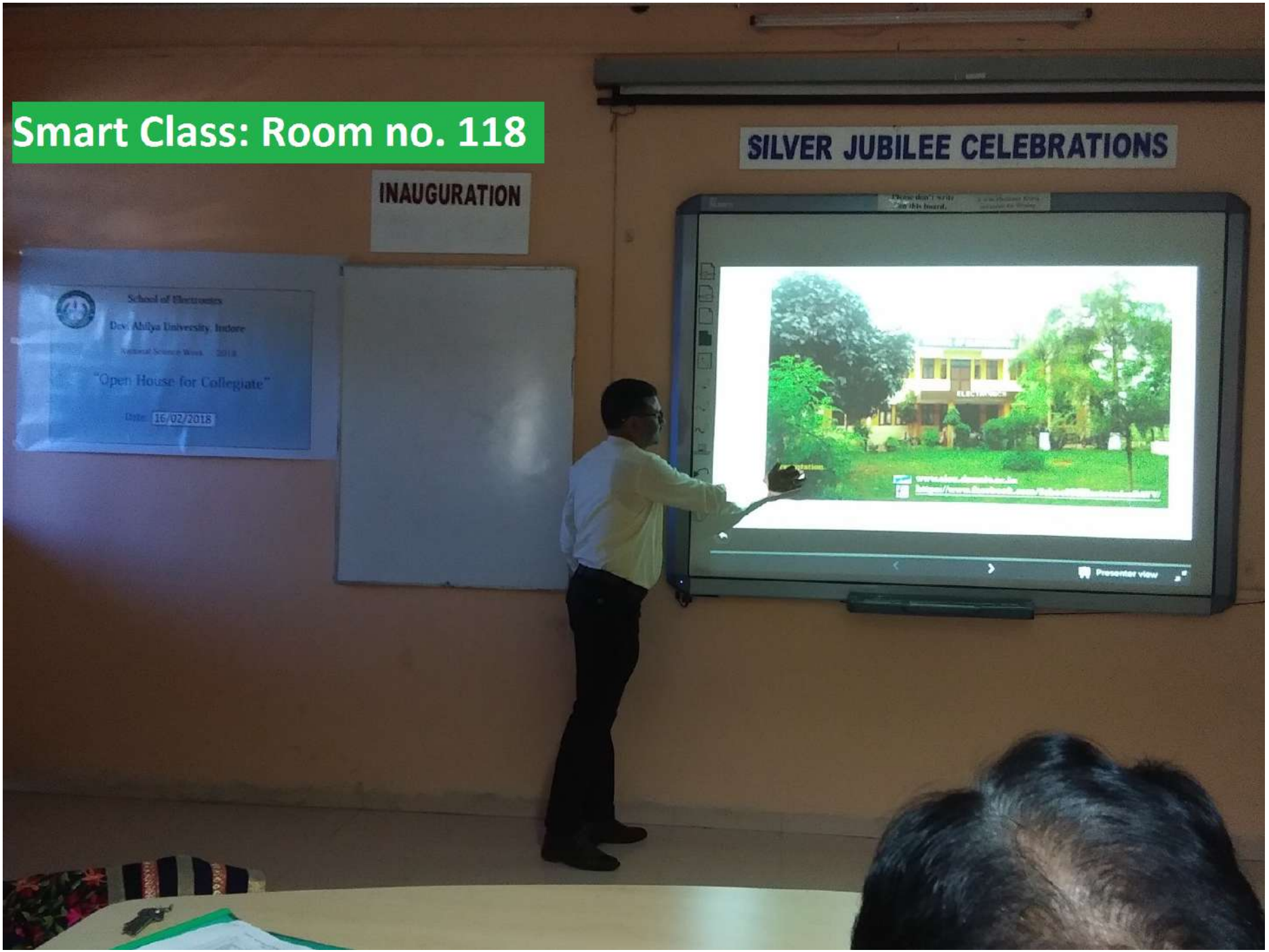
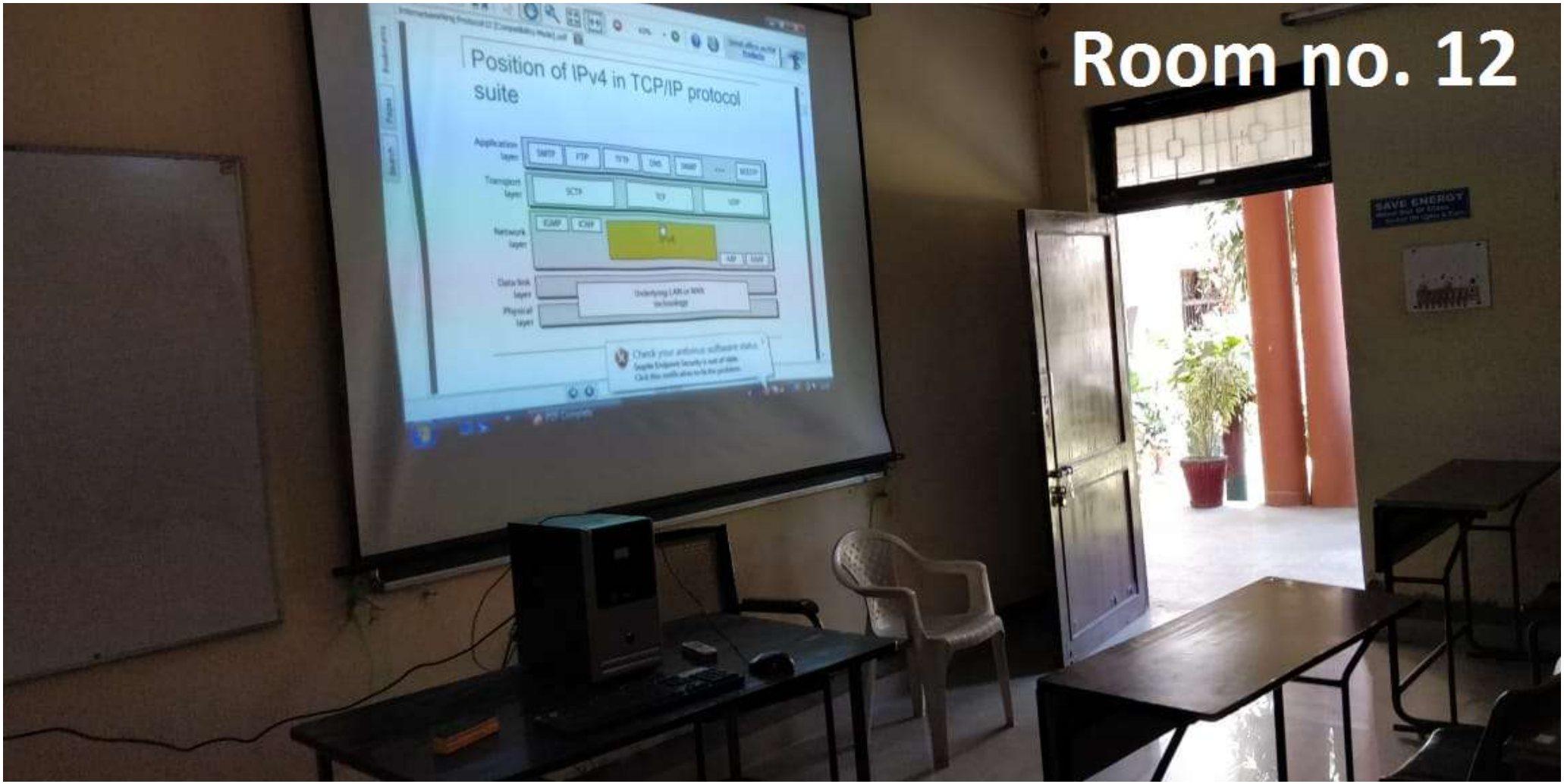
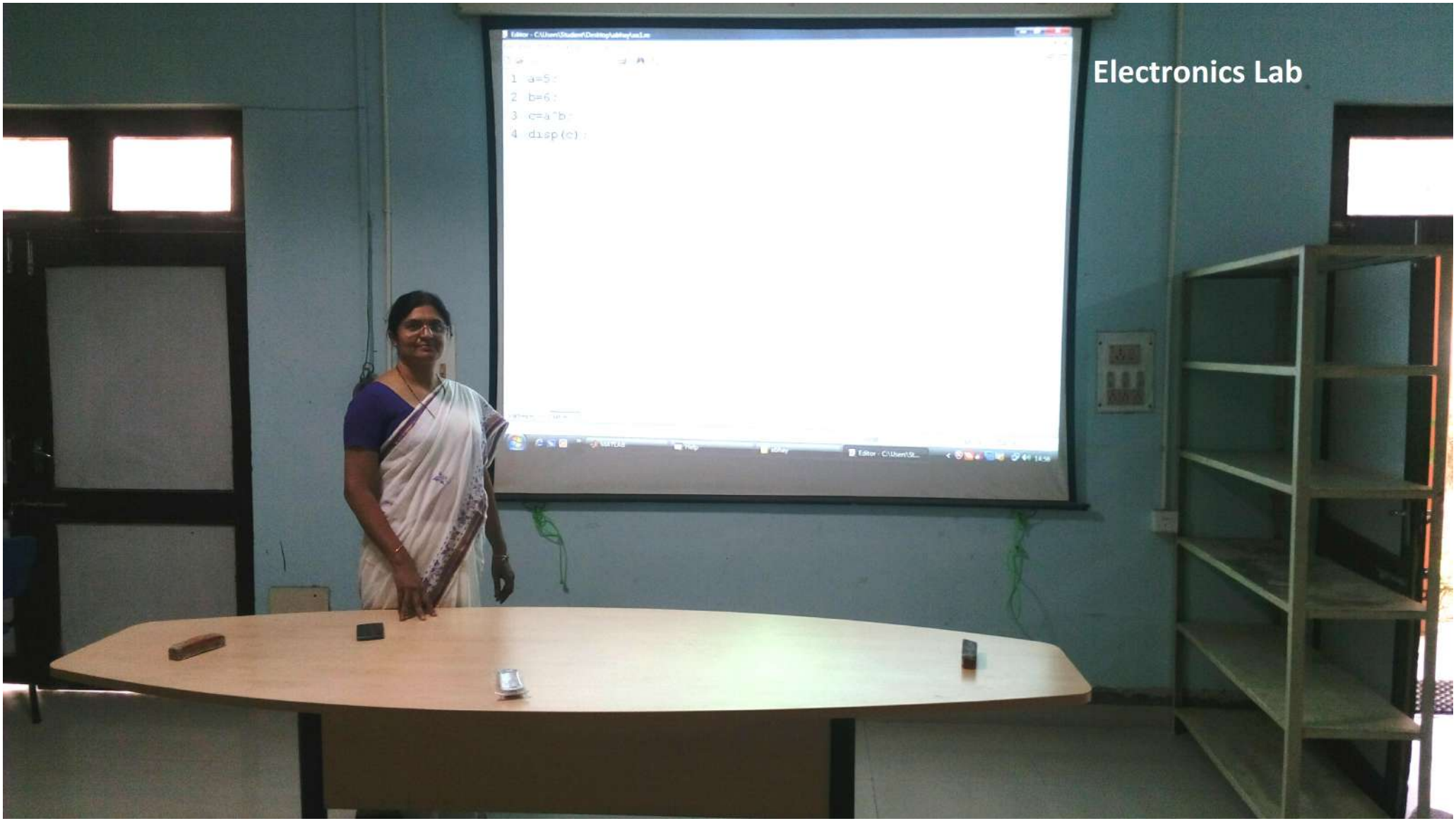

Smart Class: Room no. 118
INAUGURATION
SILVER JUBILEE CELEBRATIONS
School of Electronics
Dev. Ahilya University, Indore
"Open House for Collegiate"
Date: 16/02/2018
Presenter view


Room no. 12
Position of IPv4 in TCP/IP protocol suite
SAVE ENERGY


Room no. 13


ilya Vishwavidyalaya
ENTUPLE
School of Electronics
&
e of Engineering and Technology
Organizing
Short Term Course on
nd Layout Design Methodologies using Cadence Design Flow"
e: 8th – 12th Ja
ENTUPLE
TECHNOLOGIES
Introduction to
VLSI


1 a=5;
2 b=6;
3 c=a^b;
4 disp(c);
Electronics Lab

VLSI & Embedded Systems Laboratory