EE-9/2/2021-R&D-E
Government of India
Ministry of Electronics & Information Technology
R&D in Electronics Group
(Microelectronics Development Division)

Dated: 19.05.2023

ADMINISTRATIVE APPROVAL

Subject: Administrative Approval in respect of the project entitled "Implantable Pacemaker Chip (iPACE-CHIP)" to be implemented by IIT Indore, IIT Jammu, Institute of Engineering and Technology, Devi Ahilya Vishwavidyalaya (IET-DAVV), Indore, Shri G. S. Institute of Technology and Science SGSITS, Indore and Atal Bihari Vajpayee-Indian Institute of Information Technology and Management (ABV-IIITM), Gwalior under Chips to Startup (C2S) Programme.

I am directed to refer to Administrative Approval dated 18.05.2023 for the implementation of Programme "Chips to Startup (C2S) and to convey now the approval of the Competent Authority to the implementation of the above-mentioned project at a total estimated cost of Rs. 480.00 Lakh (Rupees Four Crore Eighty Lakh only) as grant-in-aid from Ministry of Electronics and Information Technology. The duration of the project is 5 years. The details of the project are given in the enclosed **Annexure-I**.

2. This issues with the approval of Secretary, MeitY vide computer No. 3080449 dated 03.05.2023 and concurrence of JS&FA, Ministry of Electronics & Information Technology vide computer No. 3080449 dated 03.05.2023.

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(Meenakshi Kumar)
Under Secretary to Govt. of India

1. The Pay & Accounts Office (PAO), MeitY
2. Office of the Principal Director of Audit, Finance & Communications, Civil Lines, Near Old Secretariat, Shamnath Marg, New Delhi -110 054.
3. Prof. Santosh Kumar Vishvakarma, Chief Investigator, Room Number 318, Pod 1A, Dept. of Electrical Engineering, IIT Indore, Khandwa Road, Simrol, Indore, Madhya Pradesh -453552
4. Prof. Ambika Prasad Shah, Chief Investigator, Office 1AC-629, Dept. of Electrical Engineering, IIT Jammu, Jagti, NH 44, Nagrota, Jammu -181221
5. Prof. Vaibhav Neema, Chief Investigator, E&TC Dept. IET- Devi Ahilya Vishwavidyalaya, Khandwa Road, Indore, Madhya Pradesh-452001
6. Prof. P. P. Bansod, Chief Investigator, Head, Electronics and Instrumentation Engineering Dept., Shri G. S. Institute of Technology and Science,23, Park Road, Indore, Madhya Pradesh -452003
7. Prof. Manisha Pattanaik, Chief Investigator, VLSI System Design Group, ABV-IIITM Gwalior, C Block -110, Morena Link Road, Gwalior, Madhya Pradesh -474015
8. DG(NIELIT)/CFO(NIELIT)
9. GC(SV)/GC(AKP)/Sci. 'E'(NG)/Sci. 'D'(HG)/DS(DKS), MeitY
10. Finance Division/HRD/D&D Section, MeitY
11. Master Sanction file.

Annexure-I

1	**Name of the Project**	Implantable Pacemaker Chip (iPACE-CHIP)
2	**Objective& Deliverables**	**Objective:** The objectives of the proposal can be classified as follows: • The proposed Pacemaker Chip would have pacing, sensing, EGM, Battery Measurement, telemetry and controller blocks. • The proposed blocks would be designed with reduced power, area and improved reliability. • To generate the specialized manpower in circuit and systems for Healthcare applications. • To develop startup culture in implantable biomedical devices in collaboration with consortium partners. **Deliverables of the Project:** • The proposed Implantable Pacemaker Chip (iPACE-CHIP) will be tapeout using SCL 180nm/ TSMC 130nm CMOS High Voltage, Low power, BCD PLUS. • The tested and workable iPACE-CHIP will be used in the next generation commercial product of Shree Pacetronix Ltd. with enhanced features. • Low cost SoC for Indigenous product.
3	**Year wise Milestones**	Annexure A
4	**Name of Implementing Agencies and Legal Status**	**Lead Agency:** IIT Indore (Central Government Department) **Collaborating Agencies:** 1. IIT Jammu (Central Government Department) 2. Institute of Engineering and Technology, Devi Ahilya Vishwavidyalaya, Indore (IET-DAVV Indore) (State University) 3. Shri G. S. Institute of Technology and Science, Indore (SGSITS Indore) (State Government aided) 4. Atal Bihari Vajpayee-Indian Institute of Information Technology and Management, Gwalior (ABV-IIITM Gwalior) (Central Government Department)
5.	**Total Project Duration**	5 Years Expected date of commencement: Date of 1st release of GIA Expected date of completion: 5 Years from the date of 1st release of GIA or date of completion of C2S Programme (i.e. 10.02.2027), whichever is earlier

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6. **Total Project Outlay (GEN Budget Head): Rs. 480.00 Lakh**

A. **Cumulative Budget Outlay of the Project (Year wise):**

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)					
	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
Capital Equipment	6.47	0.00	0.00	0.00	0.00	**6.47**
Consumable Stores	8.75	8.75	9.15	8.75	8.75	**44.15**
Duty on Import	0.00	0.00	0.00	0.00	0.00	**0.00**
Manpower	65.64	66.84	76.52	78.20	79.88	**367.08**
Travel & Training	7.50	7.50	7.50	7.50	7.50	**37.50**
Contingencies	4.00	4.00	4.00	4.00	4.00	**20.00**
Overheads, if any	0.90	0.90	1.00	1.00	1.00	**4.80**
Grand Total	**93.26**	**87.99**	**98.17**	**99.45**	**101.13**	**480.00**

B. **Agency wise Budget Outlay (Year Wise):**

1. IIT Indore Budget Outlay

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)					
	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
Capital Equipment	0.94	0.00	0.00	0.00	0.00	**0.94**
Consumable Stores	1.75	1.75	1.83	1.75	1.75	**8.83**
Duty on Import	0.00	0.00	0.00	0.00	0.00	**0.00**
Manpower	13.50	13.50	15.59	15.59	15.59	**73.77**
Travel & Training	1.50	1.50	1.50	1.50	1.50	**7.50**
Contingencies	0.80	0.80	0.80	0.80	0.80	**4.00**
Overheads, if any	0.18	0.18	0.20	0.20	0.20	**0.96**
Grand Total	**18.67**	**17.73**	**19.92**	**19.84**	**19.84**	**96.00**

2. Indian Institute of Technology, Jammu Budget Outlay

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)					
	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
Capital Equipment	0.94	0.00	0.00	0.00	0.00	**0.94**
Consumable Stores	1.75	1.75	1.83	1.75	1.75	**8.83**
Duty on Import	0.00	0.00	0.00	0.00	0.00	**0.00**
Manpower	13.50	13.50	15.59	15.59	15.59	**73.77**
Travel & Training	1.50	1.50	1.50	1.50	1.50	**7.50**
Contingencies	0.80	0.80	0.80	0.80	0.80	**4.00**
Overheads, if any	0.18	0.18	0.20	0.20	0.20	**0.96**
Grand Total	**18.67**	**17.73**	**19.92**	**19.84**	**19.84**	**96.00**

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3. Institute of Engineering and Technology, Devi Ahilya University, Indore Budget Outlay

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)					
	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
Capital Equipment	0.94	0.00	0.00	0.00	0.00	**0.94**
Consumable Stores	1.75	1.75	1.83	1.75	1.75	**8.83**
Duty on Import	0.00	0.00	0.00	0.00	0.00	**0.00**
Manpower	13.50	13.50	15.59	15.59	15.59	**73.77**
Travel & Training	1.50	1.50	1.50	1.50	1.50	**7.50**
Contingencies	0.80	0.80	0.80	0.80	0.80	**4.00**
Overheads, if any	0.18	0.18	0.20	0.20	0.20	**0.96**
Grand Total	**18.67**	**17.73**	**19.92**	**19.84**	**19.84**	**96.00**

4. Shri G. S. Institute of Technology and Science, Indore Budget Outlay

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)					
	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
Capital Equipment	0.94	0.00	0.00	0.00	0.00	**0.94**
Consumable Stores	1.75	1.75	1.83	1.75	1.75	**8.83**
Duty on Import	0.00	0.00	0.00	0.00	0.00	**0.00**
Manpower	13.50	13.50	15.59	15.59	15.59	**73.77**
Travel & Training	1.50	1.50	1.50	1.50	1.50	**7.50**
Contingencies	0.80	0.80	0.80	0.80	0.80	**4.00**
Overheads, if any	0.18	0.18	0.20	0.20	0.20	**0.96**
Grand Total	**18.67**	**17.73**	**19.92**	**19.84**	**19.84**	**96.00**

5. Atal Bihari Vajpayee- Indian Institute of Information Technology and Management Gwalior Budget Outlay

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)					
	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
Capital Equipment	2.71	0.00	0.00	0.00	0.00	**2.71**
Consumable Stores	1.75	1.75	1.83	1.75	1.75	**8.83**
Duty on Import	0.00	0.00	0.00	0.00	0.00	**0.00**
Manpower	11.64	12.84	14.16	15.84	17.52	**72.00**
Travel & Training	1.50	1.50	1.50	1.50	1.50	**7.50**
Contingencies	0.80	0.80	0.80	0.80	0.80	**4.00**
Overheads, if any	0.18	0.18	0.20	0.20	0.20	**0.96**
Grand Total	**18.58**	**17.07**	**18.49**	**20.09**	**21.77**	**96.00**

7. **Implementation Modalities** : IIT Indore as Lead Agency is responsible for overall implementation of the Project.

8. **Mode and extent of funding** : **As indicated below:**

(i) Budgetary Support

(a) Grants-in-aid from MeitY : Rs. 480.00 Lakh
(b) Loan : NIL

(ii) Internal generation : NIL

(iii) External Agency, if any : NIL

9. **Stages of release**

Release No.	**Pre-condition/ Stages**	**Documentation to be supplied by Implementation Agency**	**Amount to be released**
1st release	Initiation of the project	Acceptance of Terms and Conditions governing Grants-in-aid.	Rs. 18.67 Lakh (IIT Indore)
			Rs. 18.67 Lakh (IIT Jammu)
			Rs. 18.67 Lakh (IET-DAVV Indore)
			Rs. 18.67 Lakh (SGSITS Indore)
			Rs. 18.58 Lakh (ABV-IITM Gwalior)
2nd and subsequent releases	Recommendations of the PRSG & satisfactory progress report of the project	a) Submission of Utilization Certificate of the previous release. b) Technical & Financial Progress Report. **c)** Audited Statement of Accounts (at the time of Project Closure).	Rs. 77.33 Lakh (IIT Indore)
			Rs. 77.33 Lakh (IIT Jammu)
			Rs. 77.33 Lakh (IET-DAVV Indore)
			Rs. 77.33 Lakh (SGSITS Indore)
			Rs. 77.42 Lakh (ABV-IITM Gwalior)
		Total	**Rs. 480.00 Lakh**

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(Meenakshi Kumar)
Under Secretary to Govt. of India

Annexure A

Year-wise deliverables/Outcomes with specific intermediate milestones

End User: Shree Pacetronix Ltd.

Year	Quarterly Milestones	Timelines	Outcomes	Responsible Institutions
1st	• Design and verification of various sub-blocks in blocks. • **Pacing block:** ADC, DAC, Sensing: Op-Amp, Comparators • **Sensing block:** Op-amp, Filter, Comparator, Polarity Selector • **EGM block:** Op-amp, ADC • **BMM block:**Voltage Reference circuit, VCO, Counter, Comparator • **Telemetry:** Comparator • Memory • Processor design	12 months	• Sub-block development of blocks • BTech projects • MTech Thesis	IIT Indore IIT Jammu IET-DAVV Indore SGSITS Indore ABV-IIITM Gwalior Shree Pacetronix Ltd. CDAC VEGA Team
2nd	• Processor interfacing with different blocks • Tapeout of individual blocks	12 Months	• Individual Block Fabrication • Publication and Patent	IIT Indore IIT Jammu IET-DAVV Indore SGSITS Indore ABV-IIITM Gwalior Shree Pacetronix Ltd. CDAC VEGA Team
3rd	• Measurement and verification of individual blocks • Integration of various blocks	12 months	• Tapeout, Testing and Measurement • Publication and Patent	IIT Indore IIT Jammu IET-DAVV Indore

	• Tape-out for Integrated SoC (iPACE-CHIP)			SGSITS Indore ABV-IIITM Gwalior Shree Pacetronix Ltd.
4th	• Testing and verification of iPACE-CHIP • Product prototyping in Collaboration with Shree Pacetronix Ltd.	12 Months	• iPACE-CHIP Testing and Measurement • Publication and Patent • MTech and PhD Thesis • Startupt Ecosystem	IIT Indore IIT Jammu IET-DAVV Indore SGSITS Indore ABV-IIITM Gwalior Shree Pacetronix Ltd.
5th	• Clinical trial of the product • Commercialization of the product • Execution of Revenue generation model	12 Months	• Market ready pacemaker • Publication and Patent • MTech and PhD Thesis • Startupt Ecosystem	IIT Indore IIT Jammu IET-DAVV Indore SGSITS Indore ABV-IIITM Gwalior Shree Pacetronix Ltd.